ABSTRACT

A system and method for determining unmatched design elements in a circuit. The system determines instances of a first type and a second type of the design elements that are connected to a specific node in the circuit, and stores the gate signal name for each determined said occurrence of the first type of design element in a first list. The gate signal name for each determined said occurrence of the second type of design element is than stored in a second list. A value of a design element characteristic and indicia thereof for each determined said occurrence of the first and the second types of the design elements is than stored. A set difference operation is preformed on the first list and the second list to determine orphan gate signal names that appear in only one said list; and a cumulative value is determined for each said design element characteristic, by adding the design element characteristic value corresponding to each stored said orphan gate signal name, to produce a total design element characteristic value.